established. Moreover, obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is a teaching, suggestion or motivation to do so found in the references relied upon or in the knowledge generally available to one having ordinary skill in the art. However, hindsight is never an appropriate motivation for combining references and/or knowledge generally available to one having ordinary skill in the art. Accordingly, relying upon hindsight knowledge of an applicant's disclosure when the prior art does not teach nor suggest such knowledge results in the use of the invention as a template for its reconstruction.

Claim 18 includes the limitations of:

"...a semiconductor element having a circuit forming surface;

...and; a sealed confronting surface of said circuit forming surface."

In an embodiment of the invention, the confronting surface (the back side) of the circuit forming surface is sealed allowing the semiconductor device of the embodiment to be mounted to another semiconductor device without shorting. For example the confronting surface is sealed with resin 105. (Please refer to the application as filed at Fig. 1; the ultimate paragraph of page 9/38, which concludes on page 10/38; and the ultimate paragraph of page 14/38 for details of this assertion.)

The Office Action recognizes the deficiency in the Prior Art Drawings of the present application of the *sealed confronting surface of said circuit forming surface* of claim 18. Applicants assert that the Prior Art Drawings of the present application lack a teaching of at least this claimed limitation. The Office Action relies on the teachings of Ouchi, et al. for this claimed element.

Assuming arguendo that the required motivation to combine references is found, it is respectfully asserted that the reference to reference to *Ouchi, et al.* (as understood from the drawings and Derwent Abstract provided) lacks at least the claimed element of a *sealed confronting surface of said circuit forming surface*. To this end, the reference to *Ouchi, et al.* discloses electrodes 22 formed at the central portion of the circuit forming surface. *Ouchi, et al.* also discloses the use of a resin 26 along the sides of the semiconductor chip 21, but as can be plainly seen in Fig. b of *Ouchi, et al.*, an entire surface (21c) of the semiconductor chip that is confronting the circuit forming surface is exposed. In fact the Derwent Abstract provides that the sealing resin formed by moulds covers the leads (24), the circuit forming surface and the connecting device so that exposed surfaces of the external connection portion *opposite* to the circuit forming surface are exposed to the outside.

Thus, the confronting surface to the circuit forming surface of the device of *Ouchi, et al.* is exposed, an therefore is not the *sealed confronting surface of said circuit forming surface* of claim 18. Accordingly, because the reference to *Ouchi, et al.* lacks at least one of the elements of independent claim 18, and without passing on the propriety of the combination of Applicant's Prior Art Drawings and *Ouchi, et al.*, it is respectfully submitted that the rejection under 35 U.S.C.§103(a) as set forth in the Office Action is improper and should be withdrawn. Moreover, for at least the reasons set forth above the rejections over Applicant's Prior Art Drawings in view of *Ouchi, et al.* of claims 19-22 and 27, which depend immediately or ultimately from claim 18, are also believed to be improper. Withdrawal of these rejections are earnestly solicited.

Claims 23-26 have been rejected under 35 U.S.C. §103(a) as being

unpatentable over Applicant's Prior Art Drawings in view of *Ouchi, et al.* (JP 10-261753) further in view of *Hatano, et al.* (U.S. Patent 6,104,088). For at least the reasons set forth below, it is respectfully submitted that this rejection is improper and should be withdrawn.

First, it is noted that claims 23-26 depend immediately or ultimately from claim 18, which for reasons set forth above, is believed to be allowable over the applied art. As such, further discussion of the rejection of claims 23-26 is believed to be supererogatory. Nonetheless, this rejection is specifically addressed.

As stated above, the absence of one of the claimed elements in the applied art negates a proper establishment of a *prima facie* case of obviousness. Claims 23 and 25 both include the limitation that *"...the semiconductor device is mounted on another semiconductor device..."*. To wit, there are two semiconductor devices recited in these claims.

The Office Action relied on the teaching of the reference to *Hatano, et al.* for this limitation. Specifically, at page 5, the Office Action states "...Hatano discloses two semiconductor device mounted on each other where the second device has electrodes (See Figure 1).

A review of Fig. 1 of the reference *Hatano, et al.*, and its supporting disclosure reveals that a complementary wiring package 1 is mounted on a multi-layer printed wiring board (unnumbered). The multi-layer printed wiring board is sandwiched between the wiring package 1 and an integrated circuit package 4. It is noted that the complementary wiring package 1 includes no semiconductor integrated circuits.

Similarly, as shown in Fig. 2, complementary wiring package 11 includes no semiconductor integrated circuits. (Please refer to Fig. 1 and column 4, lines 1-54 of the reference to *Hatano, et al.* for support for this assertion.)

Accordingly, it is respectfully submitted that the reference to *Hatano, et al.* lacks at least the 'another semiconductor device' as is claimed. Therefore, and for at least this reason, it is respectfully asserted that the rejection of claims 23 and 25 and the claims that depend therefrom is improper and should be withdrawn.

Conclusion

For at least the reasons set forth above claims 18-27 are believed to be allowable over the applied art. Allowance thereof is earnestly solicited.

In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact William S. Francos, Esq. (Reg. No. 38,456) at (610) 375-3513 to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

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MARKED VERSION SHOWING CHANGES TO PARAGRAPH ON PAGE 8/38

Figs. 16(a)-16(c) [Fig. 16] is a flowchart showing the manufacturing process of the semiconductor element in the second embodiment.